THAT WHICH IS CLAIMED IS:

1. A method of forming an integrated circuit device, comprising the steps of:

forming a microelectronic structure on a substrate;

covering a sidewall of the microelectronic structure and a portion of the substrate with a first electrically insulating layer comprising a first material; then

covering the microelectronic structure and the first electrically insulating layer with a second electrically insulating layer comprising a second material different from the first material;

etching the second electrically insulating layer and the first electrically insulating layer in sequence to define a contact hole therein that exposes the substrate; and

widening the contact hole to expose the first electrically insulating layer by wet etching sidewalls of the contact hole using an etchant that etches the second material faster than the first material.

2. The method of Claim 1, wherein said widening step is followed by the steps of:

forming a sidewall insulating spacer on a sidewall of the contact hole; and then

etching a portion of the first electrically insulating layer extending opposite the substrate, using the sidewall insulating spacer as an etching mask.

3. The method of Claim 2, wherein the substrate comprises a polysilicon conductive plug therein; and wherein said step of etching the second electrically insulating layer and the first electrically insulating layer in sequence comprises etching the first electrically insulating layer to expose the conductive plug.

4. The method of Claim 3, wherein the first electrically insulating layer comprises silicon nitride; and wherein the second electrically insulating layer comprises silicon dioxide.

5. The method of Claim 1, wherein said step of etching the second electrically insulating layer and the first electrically insulating layer in sequence comprises dry etching the second electrically insulating and the first electrically insulating layer in sequence.

6. The method of Claim 3, wherein said dry etching step comprises dry etching the second electrically insulating and the first electrically insulating layer in sequence to expose the conductive plug.

7. A method of forming an integrated circuit memory device, comprising the steps of:

forming an electrically conductive bit line on a substrate having a first conductive plug therein extending to a surface thereof;

covering the bit line and the first conductive plug with a silicon nitride capping layer; then

covering the bit line and the silicon nitride capping layer with an electrically insulating oxide layer;

dry etching the electrically insulating oxide layer and the silicon nitride capping layer in sequence to define a contact hole therein that exposes the first conductive plug at the surface; and

widening the contact hole to expose the silicon nitride capping layer by wet etching sidewalls of the contact hole using an etchant that etches the electrically insulating oxide layer at a faster rate than the silicon nitride capping layer.

8. The method of Claim 7, wherein said widening step is followed by the steps of:

forming an oxide spacer on a sidewall of the contact hole; and then

wet etching a portion of the silicon nitride capping extending opposite the first conductive plug, using the oxide as an etching mask.

9. The method of Claim 8, wherein said step of wet etching a portion of the silicon nitride capping layer is followed by the step of forming a second conductive plug that extends in the contact hole and ohmically contacts the first conductive plug.

10. The method of Claim 7, wherein said step of forming an electrically conductive bit line comprises forming an electrically conductive bit line as a composite of a polysilicon conductive layer and a tungsten silicide layer on an upper surface of the polysilicon conductive layer.

11. The method of Claim 9, wherein said step of forming an electrically conductive bit line comprises forming an electrically conductive bit line as a composite of a polysilicon conductive layer and a tungsten silicide layer on an upper surface of the polysilicon conductive layer.

12. A method of forming an integrated circuit memory device, comprising the steps of:

forming a first interlayer insulating layer on a semiconductor substrate;

forming a first contact hole in the first interlayer insulating layer;

forming a first conductive plug in the first contact hole;

forming first and second bit lines at adjacent locations on an upper surface of the first interlayer insulating layer;

forming a capping layer that covers the first conductive plug and the first and second bit lines;

forming a second interlayer insulating layer on the capping layer;

etching the second interlayer insulating layer and the capping layer in sequence to define a second contact hole that exposes a first portion of the first conductive plug;

widening the second contact hole by selectively etching the sidewalls of the second contact hole with an etchant that etches the second interlayer insulating layer at a faster rate than the capping layer; then

forming a sidewall spacer on the sidewall of the second contact hole; and

etching the capping layer to expose a second portion of the first conductive plug that is greater than the first portion, using the sidewall spacer as an etching mask.

13. The method of Claim 12, wherein the first and second interlayer insulating layers comprise silicon dioxide; and wherein the capping layer comprises silicon nitride.

14. The method of Claim 12, wherein said step of etching the second interlayer insulating layer is preceded by the steps of:

forming a masking layer having a pilot hole therein, on the second interlayer insulating layer; and

narrowing the pilot hole by forming a pilot hole spacer on a sidewall of the first pilot hole.

15. The method of Claim 14, wherein said step of etching the second interlayer insulating layer comprises dry etching the second interlayer insulating layer through the narrowed pilot hole.

16. The method of Claim 12, wherein the second interlayer insulating layer comprises a material selected from the group consisting of undoped silicate glass (USG), borophosphosilicate glass (BPSG), phosphosilicate glass (PSG) and high temperature oxide (HTO).

17. The method of Claim 16, wherein the capping layer comprises a material selected from the group consisting of silicon nitride, nitride oxide and oxynitride.

18. The method of Claim 15, wherein the second interlayer insulating layer comprises a material selected from the group consisting of undoped silicate glass (USG), borophosphosilicate glass (BPSG), phosphosilicate glass (PSG) and high temperature oxide (HTO).

19. The method of Claim 18, wherein the capping layer comprises a material selected from the group consisting of silicon nitride, nitrided oxide and oxynitride.